IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application:
Application No.:
Filed:
Title:
Commissioner for patents
Washington, D.C. 20231

POWER OF ATTORNEY BY ASSIGNEE OF ENTIRE INTEREST
(REVOCATION OF PRIOR POWERS)

As assignee of record of each of the patent applications listed in the table of attachment A,

REVOCATION OF PRIOR POWERS OF ATTORNEY

all powers of attorney previously given in each of the listed patent applications are hereby revoked, and

NEW POWER OF ATTORNEY

the following attorneys/agents are hereby appointed to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith: I hereby appoint all attorneys of Thomas, Kayden, Horstemeyer & Risley, LLP, who are listed under the USPTO Customer Number shown below as the attorneys to prosecute this application and to transact all business in the United States Patent and Trademark Office connected therewith, recognizing that the specific attorneys listed under that Customer Number may be changed from time to time at the sole discretion of Thomas, Kayden, Horstemeyer & Risley, LLP, and request that all correspondence about the application be addressed to the address filed under the same USPTO Customer Number.

000047390
Patent Trademark Office

Please direct all future correspondence and telephone calls to:

Daniel R. McClure, Reg. No. 38,962
THOMAS, KAYDEN, HORSTEMEYER & RISLEY, L.L.P.
600 Galleria Pkwy, 15th Floor
Atlanta, GA 30339-5994
770-933-9500

ASSIGNEE OF ENTIRE INTEREST
TAIWAN SEMICONDUCTOR MANUFACTURING COMPANY, LTD.
8, Li-Hsin Rd. 6
Hsinchu Science Park
Hsinchu, Taiwan 300-77, R.O.C.

ASSIGNEE CERTIFICATION

The certification under 37 C.F.R. §3.73(b) establishing the right of assignee to take action is attached hereto along with documentation evidencing same. Further, in my official position with Taiwan Semiconductor Manufacturing Company, Ltd., I am authorized to sign documents and otherwise act on its behalf in connection with the management and handling of patent applications and other intellectual property matters.

Date: 08/15/2008

Keith A. Chanrob
Director - Intellectual Property Division

0503-A33630H-US

Attachment A

No.	TKHR Ref.	Serial No	Application Title	Filing Date	Assignment (Reel/Frame)
1.	252016-3590	07/865,412	Membrane dielectric isolation IC fabrication	04/08/1992	007470/0232
2.	252016-3600	08/478476	A contact stepper printed lithography method	06/07/1995	008461/0131
3.	252016-3610	08/484,029	Membrane dielectric isolation transistor fabrication	06/07/1995	008328/0321
4.	252016-3620	08/475,796	Membrane dielectric isolation IC fabrication	06/07/1995	008328/0327
5.	252016-3630	08/474,448	Method of forming a circuit membrane with a polysilicon film	06/07/1995	008282/0551
6.	252016-3640	08/477,785	Three dimensional semiconductor circuit structure with optical interconnection	06/07/1995	008282/0522
7.	252016-3650	08/475,770	Method of making a stacked 3D integrated circuit structure	06/07/1995	008282/0533
8.	252016-3660	08/484,144	Method of forming a multi-chip module from a membrane circuit	06/07/1995	009145/0247
9.	252016-3670	08/813,439	Membrane dielectric isolation IC fabrication	03/10/1997	008964/0585
10.	252016-3680	08/315,905	Method of making dielectrically isolation integrated circuit	09/30/1994	009459/0780
11.	252016-3690	08/472,426	Membrane dielectric isolation IC fabrication	06/07/1995	009920/0900
12.	252016-3700	08/850,749	High density three-dimensional IC interconnection	05/02/1997	009970/0647
13.	252016-3710	09/028,081	Membrane dielectric isolation IC fabrication	02/23/1998	010194/0824
14.	252016-3720	08/488,380	Electro-magnetic lithographic alignment method	06/07/1995	011989/0662
15.	252016-3730	08/779,679	Membrane dielectric isolation IC fabrication	01/07/1997	009920/0897
16.	252016-3740	09/775,597	Stress controlled dielectric integrated circuit fabrication	02/05/2001	014126/0960
17.	252016-3750	09/775,670	Stress controlled dielectric integrated circuit fabrication	02/05/2001	014106/0280
18.	252016-3760	08/483,731	Lithography device for semiconductor circuit pattern generation	06/07/1995	Recorded 007470/0232 at the parent application USP 5,354,695
19.	252016-3770	09/775,598	Membrane 3D IC fabrication	02/05/2001	Recorded 007470/0232 at the parent

					application USP 5,354,695
20.	252016-3780	10/766,629	Apparatus and methods for maskless pattern generation	01/27/2004	Recorded 007470/0232 at the parent application USP 5,354,695
21.	252016-3790	10/766,557	Method for maskless lithography	01/27/2004	Recorded 007470/0232 at the parent application USP 5,354,695
22.	252016-3800	10/385,386	Lithography device for semiconductor circuit pattern generation	03/07/2003	Recorded 007470/0232 at the parent application USP 5,354,695
23.	252016-3810	10/742,057	Membrane 3D IC fabrication	12/18/2003	Recorded 007470/0232 at the parent application USP 5,354,695
24.	252016-3820	10/460,027	Stress-controlled dielectric integrated circuit	06/11/2003	015815/0978
25.	252016-3830	10/460,483	Stress-controlled dielectric integrated circuit	06/11/2003	015818/0552
26.	252016-3840	10/665,757	Method of making an integrated circuit	06/11/2003	Recorded 007470/0232 at the parent application USP 5,354,695
27.	252016-3850	10/700,429	Membrane IC fabrication	11/03/2003	Recorded 007470/0232 at the parent application USP 5,354,695
28.	252016-3860	10/742,282	Membrane 3D IC fabrication	12/19/2003	Recorded 007470/0232 at the parent application USP 5,354,695
29.	252016-3870	10/971,341	Flexible and elastic dielectric integrated circuit	10/22/2004	Recorded 007470/0232 at the parent application USP 5,354,695

30.	252016-3880	10/741,647	Membrane 3D IC fabrication	12/18/2003	Recorded 007470/0232 at the parent application USP 5,354,695
31.	252016-3890	11/042,581	Lithography device for semiconductor circuit pattern generation	01/24/2005	Recorded 007470/0232 at the parent application USP 5,354,695
32.	252016-3900	12/009,581	Flexible and elastic dielectric integrated circuit	01/18/2008	Recorded 007470/0232 at the parent application USP 5,354,695